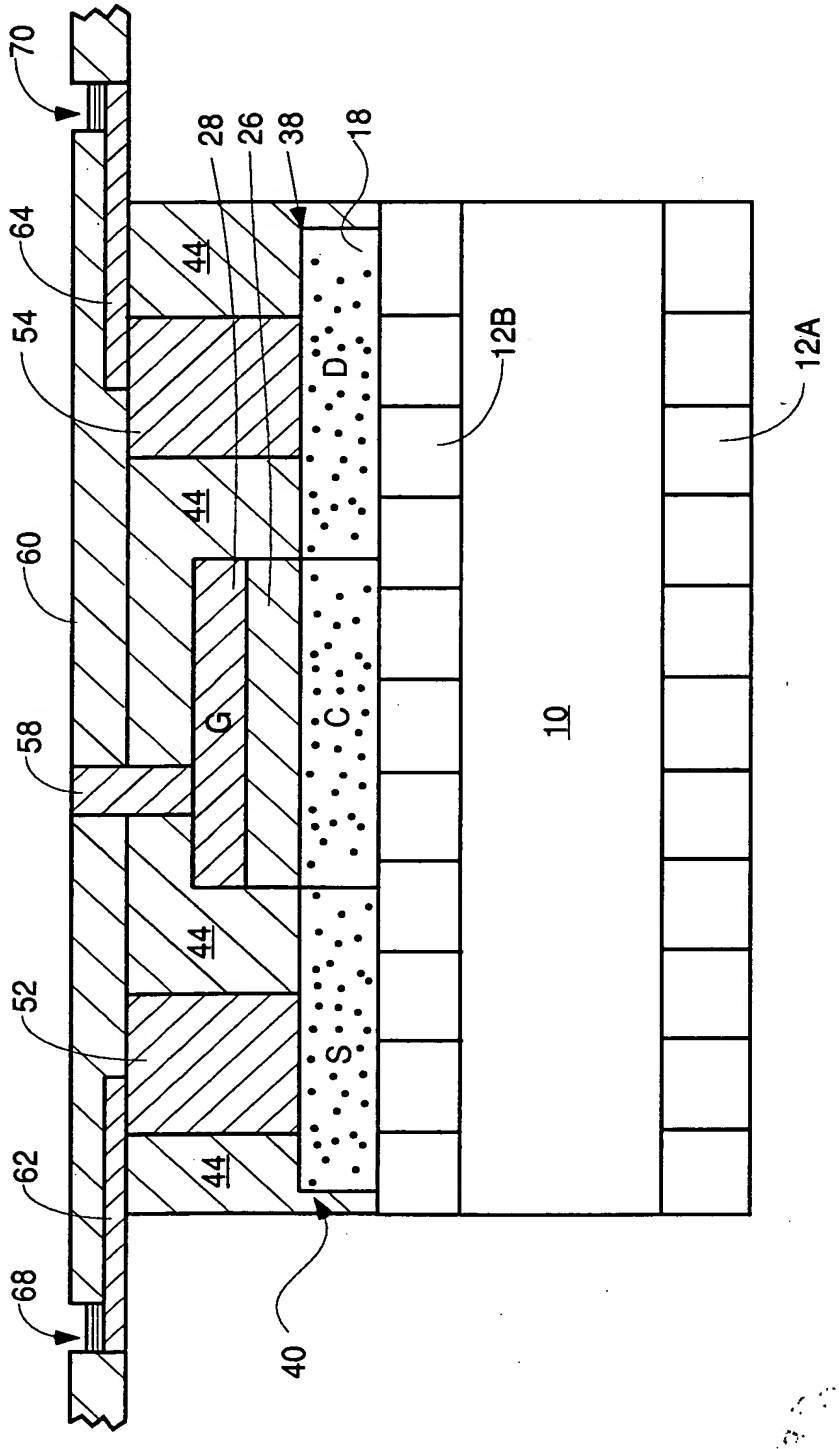


FIG. 1

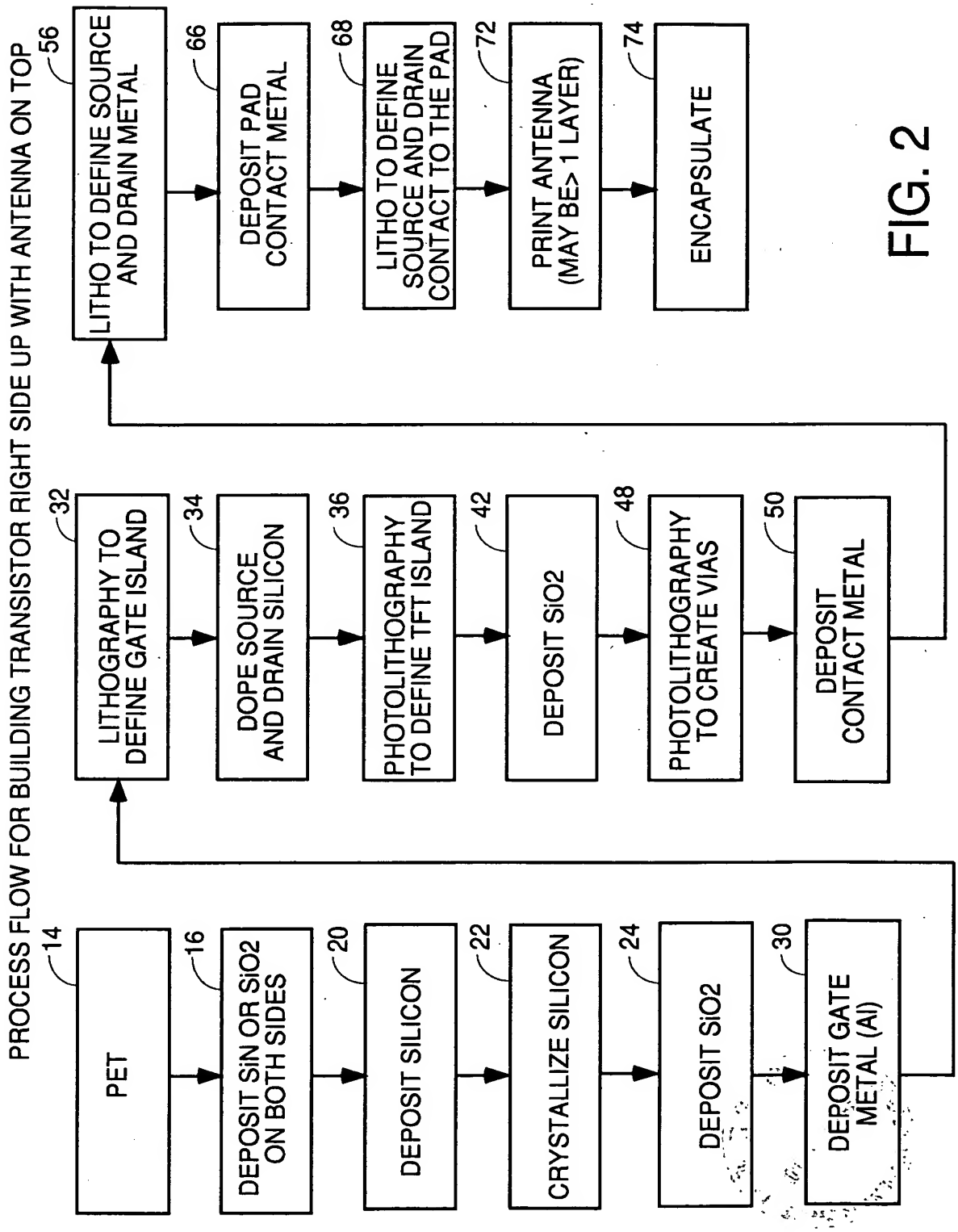
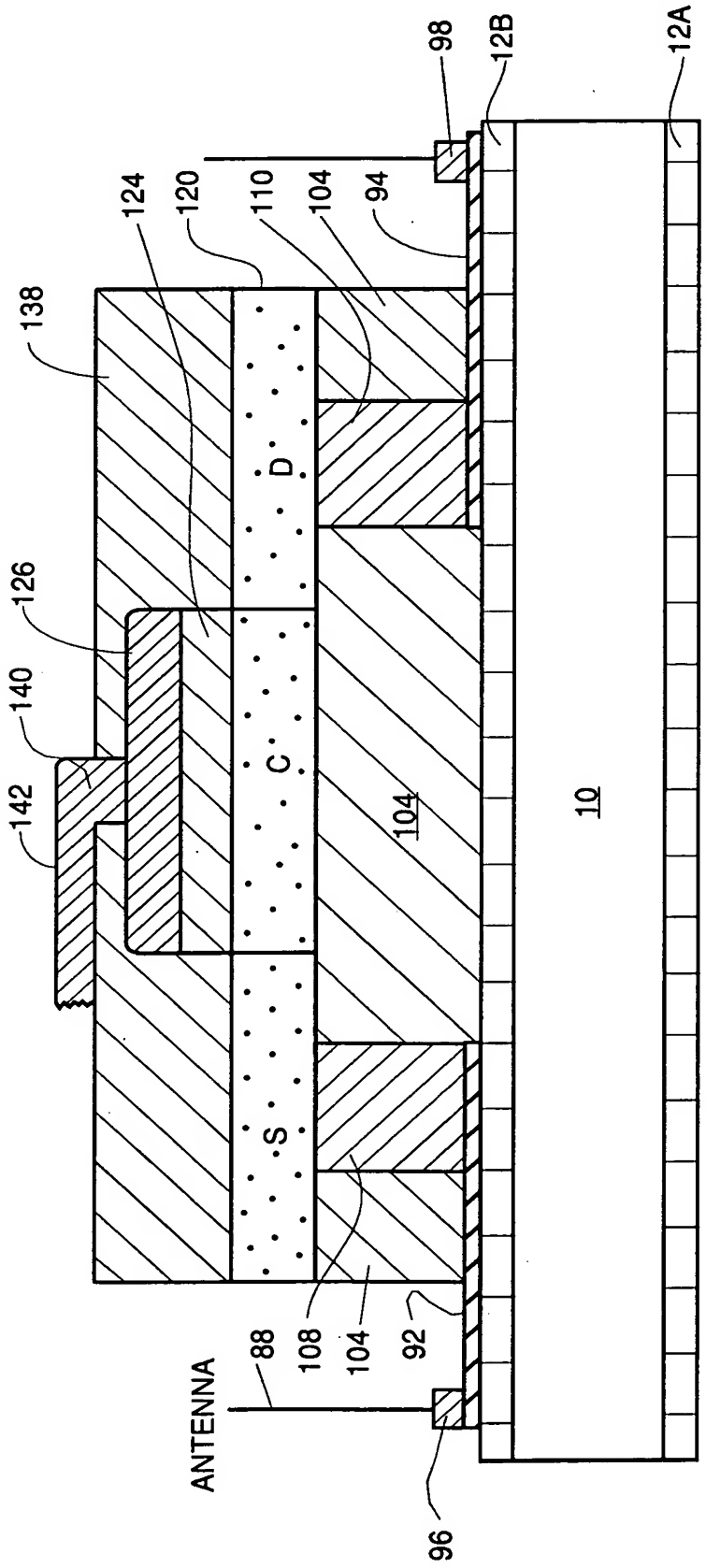

PROCESS FLOW FOR BUILDING TRANSISTOR RIGHT SIDE UP WITH ANTENNA ON TOP
14
PET
16
DEPOSIT SiN OR SiO2 ON BOTH SIDES
20
DEPOSIT SILICON
22
CRYSTALLIZE SILICON
24
DEPOSIT SiO2
30
DEPOSIT GATE METAL (Al)
32
LITHOGRAPHY TO DEFINE GATE ISLAND
34
DOPE SOURCE AND DRAIN SILICON
36
PHOTOLITHOGRAPHY TO DEFINE TFT ISLAND
42
DEPOSIT SiO2
48
PHOTOLITHOGRAPHY TO CREATE VIAS
50
DEPOSIT CONTACT METAL
56
LITHO TO DEFINE SOURCE AND DRAIN METAL
66
DEPOSIT PAD CONTACT METAL
68
LITHO TO DEFINE SOURCE AND DRAIN CONTACT TO THE PAD
72
PRINT ANTENNA (MAY BE> 1 LAYER)
74
ENCAPSULATE

FIG. 2



UPSIDE DOWN TRANSISTOR ON TOP OF PRINTED ANTENNA

FIG. 3

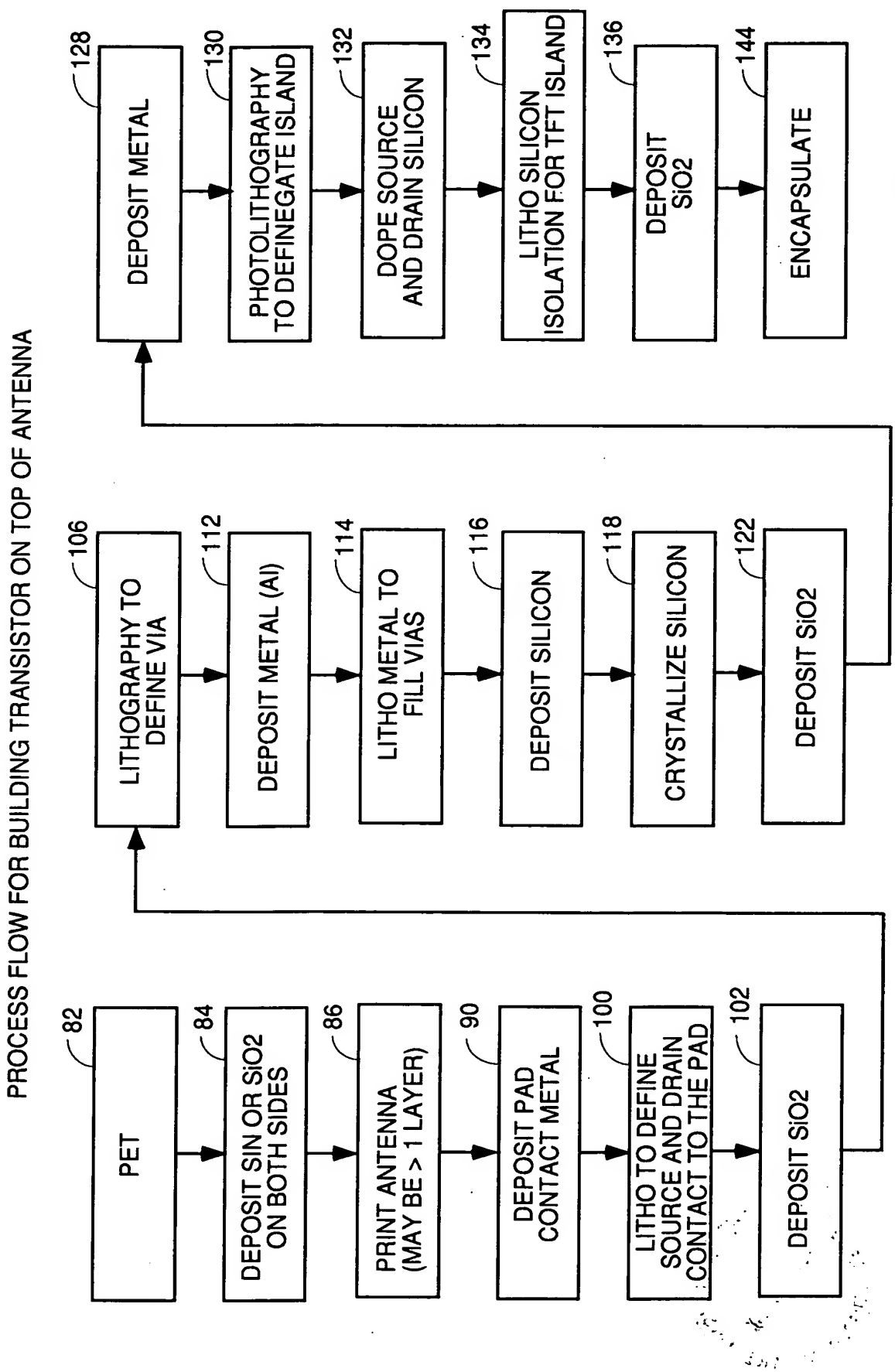

PROCESS FLOW FOR BUILDING TRANSISTOR ON TOP OF ANTENNA
82
PET
84
DEPOSIT SIN OR SiO2 ON BOTH SIDES
86
PRINT ANTENNA (MAY BE > 1 LAYER)
90
DEPOSIT PAD CONTACT METAL
100
LITHO TO DEFINE SOURCE AND DRAIN CONTACT TO THE PAD
102
DEPOSIT SiO2
106
LITHOGRAPHY TO DEFINE VIA
112
DEPOSIT METAL (Al)
114
LITHO METAL TO FILL VIAS
116
DEPOSIT SILICON
118
CRYSTALLIZE SILICON
122
DEPOSIT SiO2
128
DEPOSIT METAL
130
PHOTOLITHOGRAPHY TO DEFINEGATE ISLAND
132
DOPE SOURCE AND DRAIN SILICON
134
LITHO SILICON ISOLATION FOR TFT ISLAND
136
DEPOSIT SiO2
144
ENCAPSULATE

FIG. 4

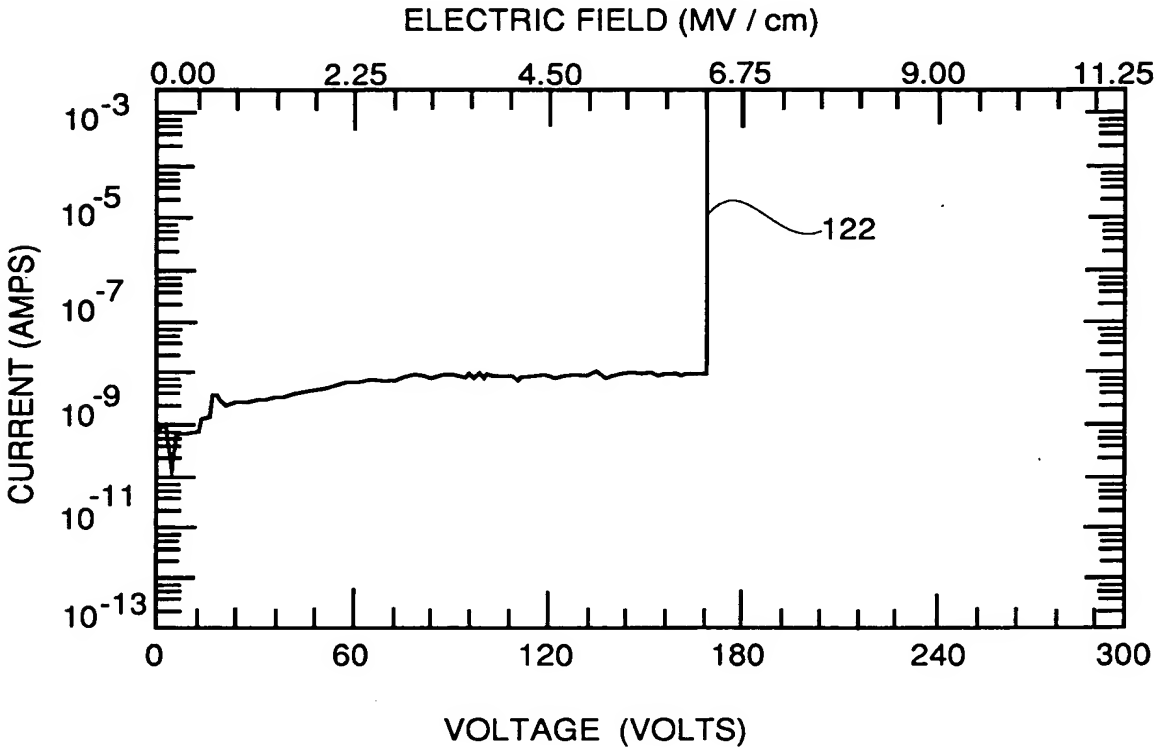


FIG. 5

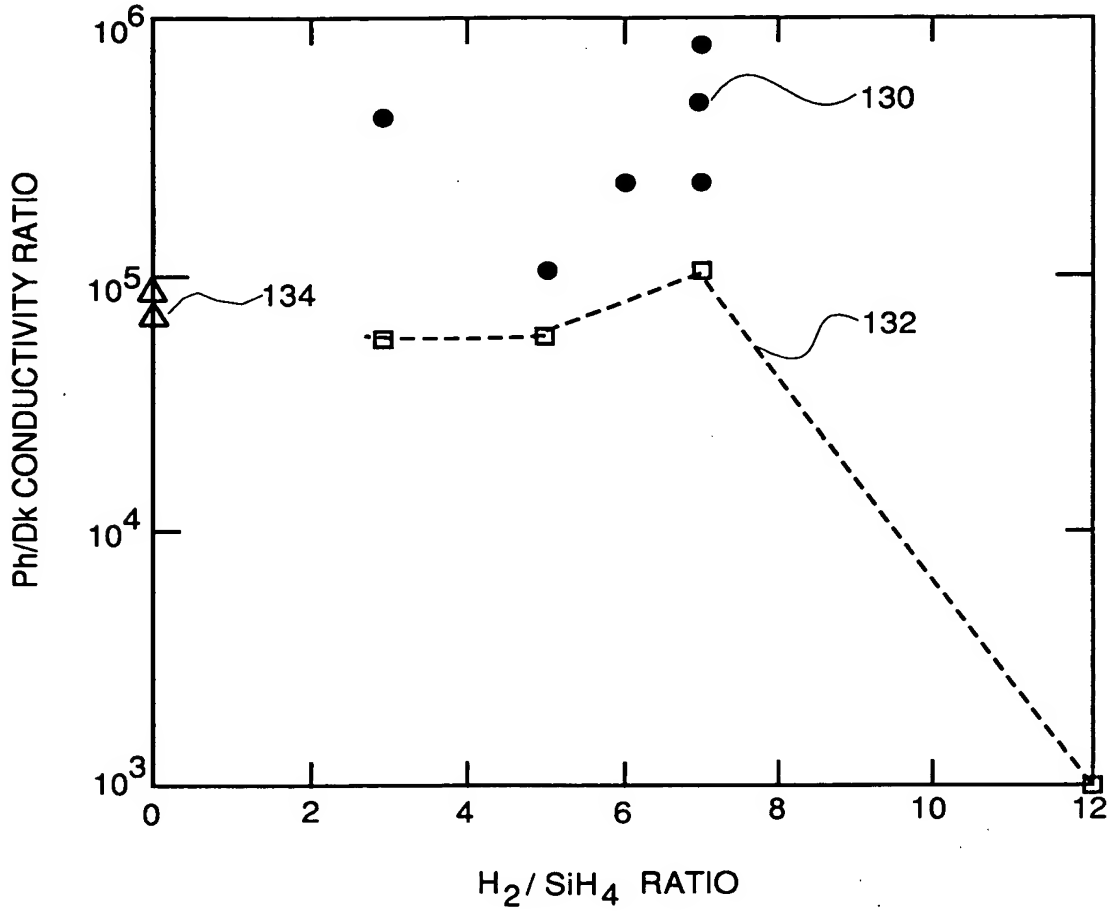

Ph/Dk CONDUCTIVITY RATIO
10^6
10^5
10^4
10^3
130
134
132
0
2
4
6
8
10
12
H_2/SiH_4 RATIO

FIG. 6

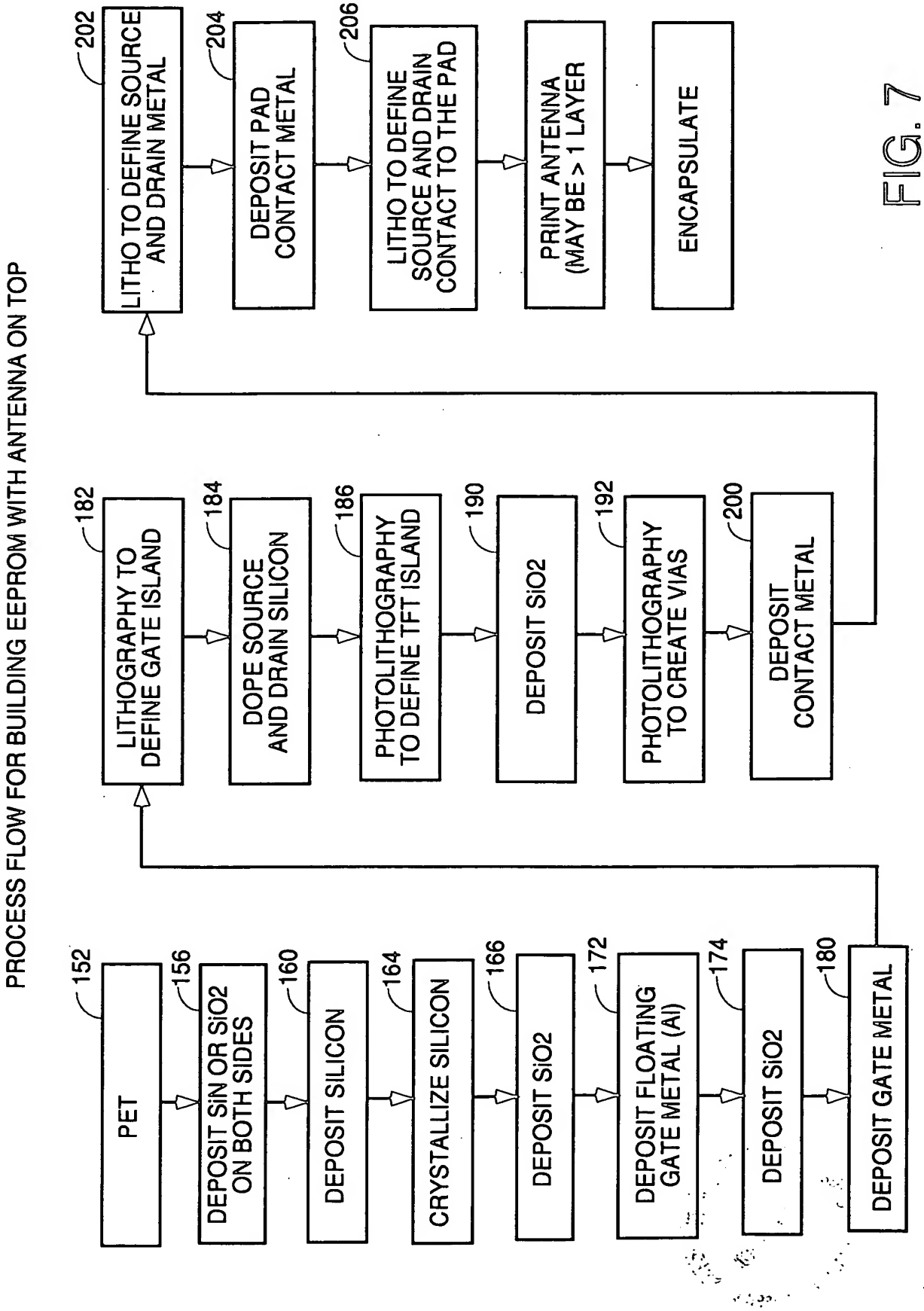

PROCESS FLOW FOR BUILDING EEPROM WITH ANTENNA ON TOP
152
PET
156
DEPOSIT SiN OR SiO2 ON BOTH SIDES
160
DEPOSIT SILICON
164
CRYSTALLIZE SILICON
166
DEPOSIT SiO2
172
DEPOSIT FLOATING GATE METAL (Al)
174
DEPOSIT SiO2
180
DEPOSIT GATE METAL
182
LITHOGRAPHY TO DEFINE GATE ISLAND
184
DOPE SOURCE AND DRAIN SILICON
186
PHOTOLITHOGRAPHY TO DEFINE TFT ISLAND
190
DEPOSIT SiO2
192
PHOTOLITHOGRAPHY TO CREATE VIAS
200
DEPOSIT CONTACT METAL
202
LITHO TO DEFINE SOURCE AND DRAIN METAL
204
DEPOSIT PAD CONTACT METAL
206
LITHO TO DEFINE SOURCE AND DRAIN CONTACT TO THE PAD
PRINT ANTENNA (MAY BE > 1 LAYER
ENCAPSULATE

FIG. 7

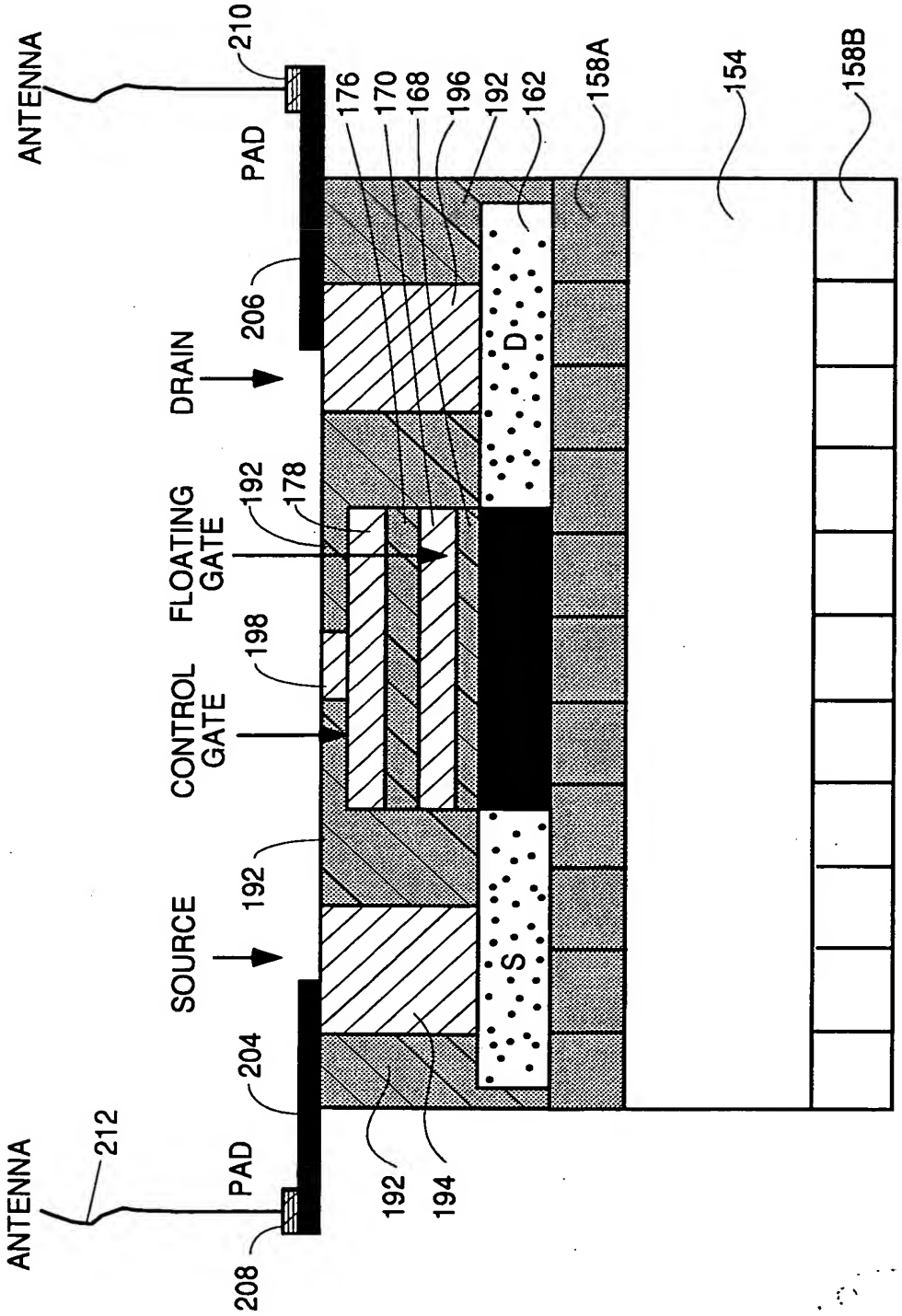


FIG. 8

SCHEMATIC OF A SINGLE EEPROM BUILT ON PET WITH THE CONTACT PADS AND THE ANTENNA PRINTED ON TOP OF THE TRANSISTOR; GATE WILL BE CONNECTED TO THE TRANSISTORS (IN ACTUAL DEVICES MULTIPLE TRANSISTORS AND EEPROM WILL BE CONNECTED TO THE CONTACT PADS)

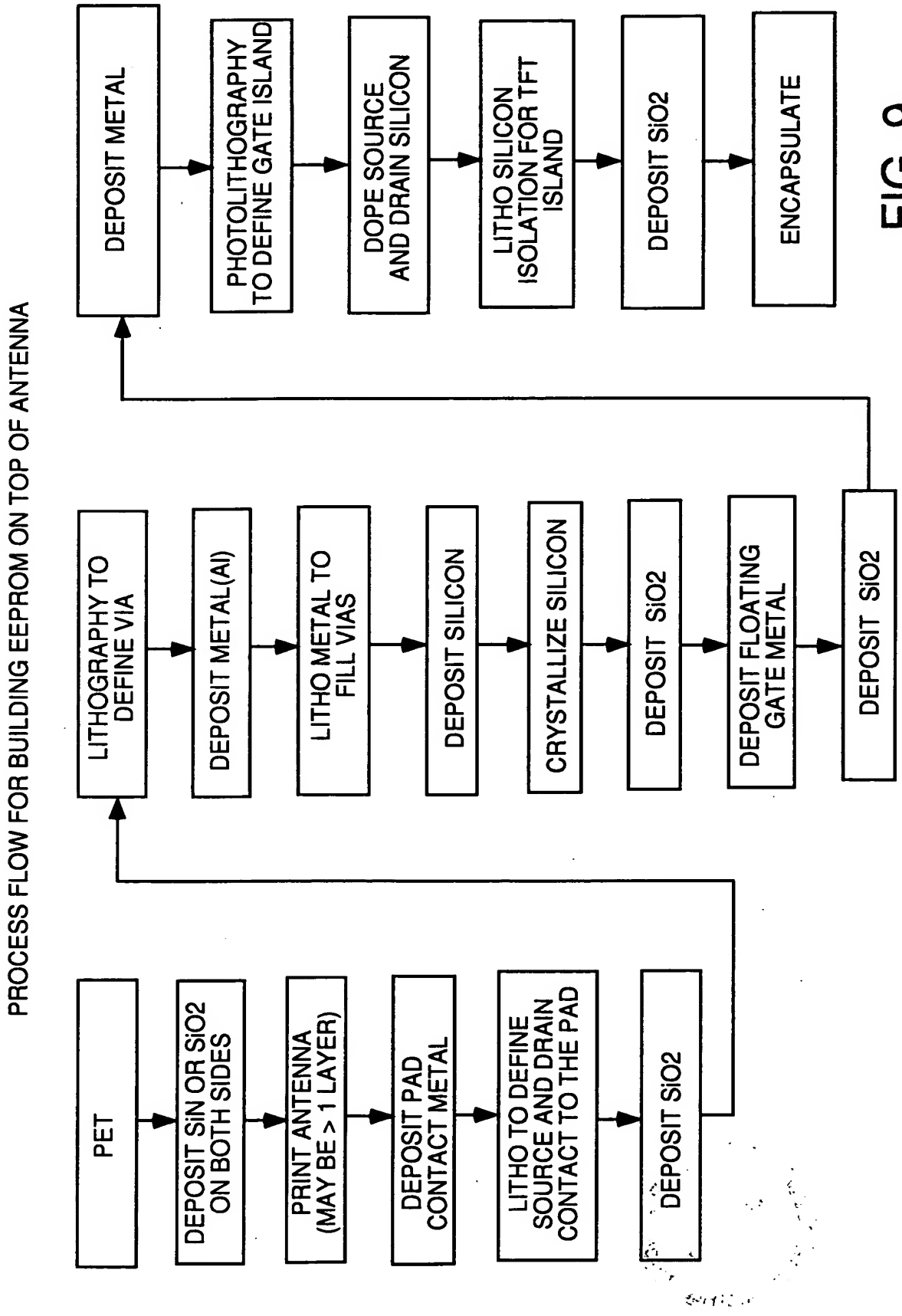
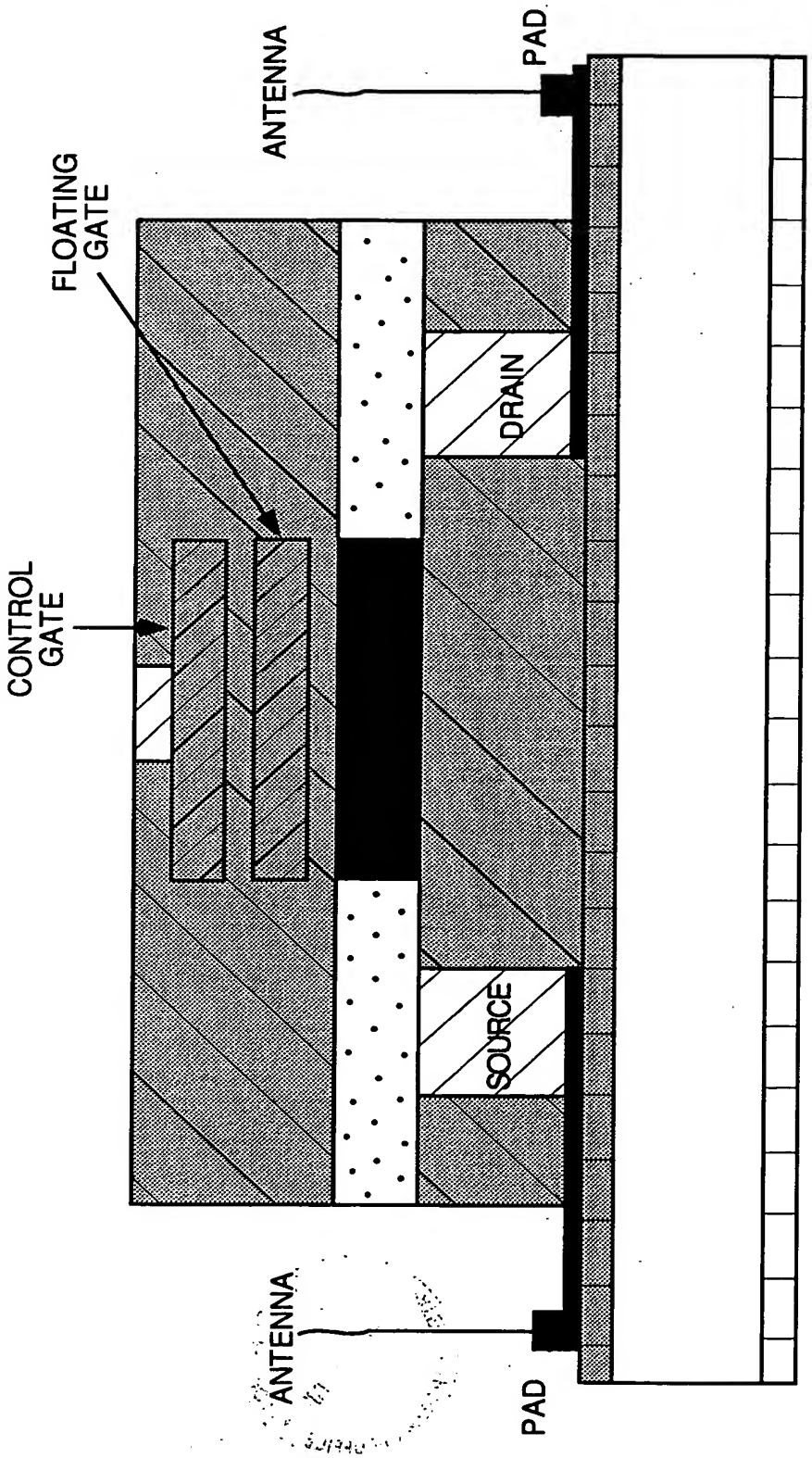

PROCESS FLOW FOR BUILDING EEPROM ON TOP OF ANTENNA
PET
DEPOSIT SiN OR SiO2 ON BOTH SIDES
PRINT ANTENNA (MAY BE > 1 LAYER)
DEPOSIT PAD CONTACT METAL
LITHO TO DEFINE SOURCE AND DRAIN CONTACT TO THE PAD
DEPOSIT SiO2
LITHOGRAPHY TO DEFINE VIA
DEPOSIT METAL(Al)
LITHO METAL TO FILL VIAS
DEPOSIT SILICON
CRYSTALLIZE SILICON
DEPOSIT SiO2
DEPOSIT FLOATING GATE METAL
DEPOSIT SiO2
DEPOSIT METAL
PHOTOLITHOGRAPHY TO DEFINE GATE ISLAND
DOPE SOURCE AND DRAIN SILICON
LITHO SILICON ISOLATION FOR TFT ISLAND
DEPOSIT SiO2
ENCAPSULATE

FIG. 9



SCHEMATIC OF A SINGLE EEPROM BUILT ON TOP OF THE PRINTED ANTENNA
(IN ACTUAL DEVICES EEPROM AND MULTIPLE TRANSISTORS WILL BE CONNECTED TO THE CONTACT PADS)

FIG. 10